#11

Appeal Brief
J. Robinson

IN THE UNITED STATES PATENT ANDTRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appellant: Stephen Skala *et al.*
Serial No. 09/874,606
Filed: June 5, 2001
For: Pad Metallization Over Active Circuitry

Patent Application
Group: 2811
Examiner: Junghaw Im

APPEAL BRIEF

Assistant Commissioner for Patents & Trademarks
Washington, DC 20231

Sir:

This is an Appeal Brief submitted pursuant to 37 CFR §1.1.92 for the above-referenced patent application and is being filed in triplicate.

I. REAL PARTY IN INTEREST

The real party in interest is Koninklijke Philips Electronics NV (KPENV); a corporation organized under the laws of The Netherlands. The patent application had been assigned to VLSI Technology, Inc. (VLSI); a corporation organized under the laws of the State of Delaware and having a principal place of business in San Jose, California. VLSI had been acquired by KPENV in June of 1999 through its sister division, Philips Electronics North America Corporation.

05/[illegible] ASMITH 00000001 141270 09874606
01 FC:1402 330.00 CH

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

III. STATUS OF CLAIMS

Claims 1 – 20 are being appealed.

Received from <408 4749082> at 5/16/03 12:45:01 PM [Eastern Daylight Time]

IV. STATUS OF AMENDMENTS

In response to the first Office action dated June 5, 2002, Appellant filed a Response and Amendment dated September 3, 2002, amending claims. In response to a second Final Office Action dated December 4, 2002, Appellant filed a Response dated February 3, 2003, amending claims.

An Advisory Action dated February 25, 2003 indicated the After Final Response did not place the application in condition for allowance. In response to the Advisory Action, Appellant filed a Notice of Appeal on September 17, 2002 and is now presenting this Appeal Brief.

The claims as finally amended are attached hereto as an Appendix.

V. SUMMARY OF INVENTION

Appellant's invention is directed to semiconductor devices and their fabrication particularly, their manufacture involving techniques for forming circuitry. One aspect of semiconductor manufacture includes the formation of bond pads on a chip. The bond pads are normally placed on the periphery of the semiconductor chip, without underlying circuitry, and are used for subsequent wire bonding to a wafer. However, it is desirable to form bond pads over active circuitry in order to reduce the size of the chip.

In an example embodiment of the present invention, a metal bond pad is formed on a semiconductor chip. The metal bond pad has a first metal pad layer, a TiN diffusion layer over the first metal pad layer, and a second metal pad layer over the TiN diffusion layer. A passivation layer is formed over the pad and subsequently etched to expose the second metal pad layer

In another example embodiment of the present invention, a system is arranged for manufacturing a semiconductor chip having a metal bond pad over active circuitry. A first metal deposition arrangement is adapted to deposit a metal bond pad on the circuit side, and a second metal deposition arrangement is adapted to deposit a metal layer over the circuit side. After the metal layer is deposited, a photoresist deposition arrangement is adapted to pattern a photoresist mask over the metal layer, and an etching arrangement is adapted to etch the circuit side and remove the portion of the metal layer not masked

Received from < 408 4749082 > at 5/16/03 12:45:01 PM [Eastern Daylight Time]

with the photoresist. When the circuit side has been etched, a photoresist removal arrangement is adapted to remove the photoresist.

VI. ISSUES FOR REVIEW

Claims 1 – 4, 15, and 16 stand rejected under 35 U.S.C. §103(a) as being unpatentable over *Bourg, Jr. et al.* (US 5,424,581 hereinafter *Bourg*) in view of *Greer* (US 6,451,681 hereinafter *Greer*).

Claims 5 – 8, 10, 11, and 14 stand rejected under 35 U.S.C. §103(a) as being unpatentable over *Bourg, Jr. et al.* (US 5,424,581) and *Greer* (US 6,451,681) in further view of *Camilletti et al.* (US 5,693,565, hereinafter *Camilletti*).

Claim 9 stands rejected under 35 U.S.C. §103(a) as being unpatentable over *Bourg, Jr. et al.* (US 5,424,581), *Greer* (US 6,451,681), and *Camilletti et al.* (US 5,693,565) in view of *Shangguan et al.* (US 6,082,610 hereinafter *Shangguan*).

Claims 7, 12, 13, and 16 –20 have been rejected however, no specific statement of rejection has been made in connection with them.

The issues are a follows:

1. **Has the Examiner met the criteria for establishing a prima facie case of obviousness in presenting the above combinations of references?**
2. **May the rejection of claims be sustained where the Examiner has failed to present any specific reason for the rejection?**

VII. GROUPING OF CLAIMS

The claims as now presented stand and fall together.

VIII. ARGUMENT

A. Scope and Content of the Prior Art.

Bourg relates to semiconductor fabrication process is provided which creates a bond pad structure that minimizes cratering of the bond pad by including an etch stop layer between the dielectric or polycrystalline silicon layer and the field oxide to avoid damage to the field oxide during removal of the dielectric or polycrystalline silicon from under the bond pad. With the use of an etch stop, the field oxide layer is not damaged during the etching process of the first dielectric layer. Moreover, a stronger bond pad structure

Received from < 408 4749082 > at 5/16/03 12:45:01 PM [Eastern Daylight Time]

which avoids cratering is formed by having first metal layer directly over the structurally stronger etch stop layer, rather than over the weaker structure of the dielectric or polycrystalline silicon layer.

Greer is concerned with a mostly copper-containing interconnect overlies a semiconductor device substrate, and a transitional metallurgy structure that includes an aluminum-containing film contacts a portion of the mostly copper-containing interconnect. In one embodiment, the transitional metallurgy is formed over a portion of a bond pad. In an alternative embodiment, the transitional metallurgy includes an energy alterable fuse portion that electrically contacts two conductive regions and, and in yet another embodiment, the transitional metallurgy is formed over a copper-containing edge seal portion.

Camilletti . is directed to a semiconductor integrated circuit chip or die more suitable in testing as an unpackaged die. A semiconductor integrated circuit (IC) die is made with enhanced resilience to handling, testing, and storage, associated with its qualification and distribution as a KNOWN GOOD DIE (KGD). The IC device has a mechanically tough and chemically inert top layer to protect it from damage. The device contacts are made of thin film metals which facilitate reversible electrical connections used in KGD testing. The overall contact structure protects the device from irreversible damage during the connection, test, and disconnection sequence.

Shangguan deals with a method which utilizes flip chip technology to provide interconnection between printed circuit boards and integrated circuits is disclosed. The method involves metallization of the bond pad and multiple, novel bump compositions and coating compositions to provide an interconnection which is reliable and which withstands differences in the coefficient of thermal expansion between the silicon device and the bump material.

Received from < 408 4749082 > at 5/16/03 12:45:01 PM [Eastern Daylight Time]

B. Discussion of the Issues.

1. The Examiner has not met the criteria for establishing a prima facie case of obviousness in presenting the above combinations of references.

Claims 1 – 4, 15, and 16

Appellant respectfully asserts the Section 103(a) rejections of all of the claims because the Examiner failed to meet all of the criteria for establishing a *prima facie* case of obviousness. To establish a *prima facie* case of obviousness, three basic criteria must be met, as indicated in the M.P.E.P. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the prior art reference (or references when combined) must teach or suggest all the claimed limitations. In this instance, the Examiner failed to meet the first and second criteria and, therefore, no *prima facie* case of obviousness has been established, as discussed below.

In regard to the third criteria above, the Final Office Action fails to cite portions of the references that teach or suggest all the limitations in the rejected claims. As the Examiner acknowledges on page 3 of the Office Action, the *Bourg* reference fails to show a diffusion barrier layer. However, in an attempt to modify the *Bourg* reference to include a diffusion barrier layer, the Examiner has not shown how the asserted modification of the *Bourg* reference would result in a structure as claimed in the instant application. For example, the Examiner has not asserted, nor can the Applicant ascertain, any portion of the cited references that teaches or suggests the limitations in claim 1 directed to "a metal layer over the ... diffusion barrier layer, and at least partially over, and in contact with, a portion of the passivation material not over the diffusion barrier layer." Upon brief review of FIG. 3 and other cited portions of the *Bourg* reference, it would appear that placing a diffusion layer on the metal layer 15 would result in the metal layer 25 being only over portions of the passivation layer that are also over the

Received from < 408 4749082 > at 5/16/03 12:45:01 PM [Eastern Daylight Time]

diffusion layer. Therefore, none of the metal layer 25 would be over a portion of the passivation material that is not over the diffusion barrier layer. For instance, placing a diffusion layer over the entire surface of the metal layer 15 (corresponding to the metal film 200 over the bond-pad 128 in the *Greer* reference) would result in the passivation 22 below the metal layer 25 also being over the added diffusion layer. Therefore, the asserted modification of the '581 reference fails to teach the claimed limitations recited above.

In further regard to the third criteria above, the Examiner has mistakenly interpreted various portions of the cited references. For instance, the Examiner mistakenly asserts that passivation material 300 is a diffusion barrier layer, which is contrary to the teachings in the '*Greer* reference (*see, e.g.*, column 4, lines 14-36). In addition, the Examiner's assertion that the metal film 200 (asserted to be a "diffusion barrier") is "arranged to mitigate inter-metallic aluminum-based compounds forming" is unsupported by the cited portion of the '*Greer* reference. Specifically, the cited portion of the '681 reference including column 3, lines 61-67 fails to discuss any mitigation of inter-metallic aluminum-based compounds forming by the metal film 200.

In regard to the first and second criteria above, Applicant submits that the asserted modification of the *Bourg* reference would render the reference unsatisfactory for its intended purpose. Relevant case law indicates that, where an asserted modification of a primary reference would render that reference unsatisfactory for its intended purpose, there is no motivation to make the modification (*see, e.g., In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed.Cir. 1984). In this instance, the asserted modification of the *Bourg* reference to include a diffusion layer between the first metal layer 15 and the second metal layer 25 would defeat the purpose of the *Bourg* reference that includes "a stronger bond pad structure which avoids cratering." *See, e.g.*, column 2, lines 45-59. Moreover, it is unclear as to what effect removing the second metal layer 25 from the first metal layer 15 and placing a diffusion layer therebetween would have on the structure. The Examiner failed to show how the invention of the '581 reference would work were such a diffusion layer placed between the metal layers 15 and 25.

In further regard to the first criteria above, the Office Action failed to cite any evidence of motivation found in the prior art for making the asserted modifications of the

Received from < 408 4749082 > at 5/16/03 12:45:01 PM [Eastern Daylight Time]

Bourg reference. Relevant case law indicates that, without such evidence of motivation, the Section 103(a) rejection should be removed (*see, e.g., In re Dembiczak*, 175 F.3d 994, 50 USPQ2d 1614 (Fed. Cir. 1999). In this instance, the Office Action failed to cite evidence of motivation for adding the diffusion barrier layer to the structure in FIG. 3 of the *Bourg* reference; rather, the only motivation asserted by the examiner is directed to problems discussed in the secondary *Greer* reference. For example, the cited portion of the '681 reference makes no mention of problems associated with the *Bourg* reference and thus fails to discuss why one of skill in the art would be motivated to modify the *Bourg* reference. The Examiner has fails to cite evidence that shows why one skilled in the art would look to the problems cited in the '681 reference to overcome any problem in the *Bourg* reference. Specifically, Appellant submits that the Examiner has failed to show that any diffusion problem exists in connection with the *Bourg* reference and, therefore, the addition of a diffusion barrier would serve no apparent purpose. Referring to the portion of the *Greer* reference to which the Examiner refers for motivation (column 3, lines 43-46), the metal film 200 is added only "when it is *necessary* to improve adhesion" (emphasis added). Applicant submits that the Examiner has failed to discuss and show how this metal film would be necessary in connection with the *Bourg* reference or even to assert that it would be necessary to improve adhesion between the metal layers of the instant invention.

MPEP §2143.01 provides:

> **There mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. In re Mills, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990)**

Claims 5 – 8, 9, 10, 11, and 14

The § 103(a) rejection of claims 5 – 8, 10,11 and 14 are improper because the cited *Camilletti* reference fails to establish a *prima facie* case of obviousness of the claims alone or in combination with *Bourg* and *Greer*. Specifically, Appellant fails to see among the cited portions of the reference, *inter alia*, features completely corresponding to the claimed limitations of at least two entire sides of the diffusion layer being insulated by the passivation material, and a metal layer at least partially over, and in contact with, a

Received from < 408 4749082 > at 5/16/03 12:45:01 PM [Eastern Daylight Time]

portion of the passivation material not over the diffusion barrier layer. Therefore, the cited reference fails to establish a *prima facie* case of obviousness alone or in combination with those previously cited.

With particular respect to claim 10, Applicant also fails to see how the *Camilletti.* reference teaches the metal bond pad and the metal layer including the same type of metal. The cited portion of the reference (col. 8, line 8-14) provides:

> . . . bond pad 11A can be sealed by covering it with a non-corroding conductive metal layer 16A, although in some cases, a corrodible material can be employed. Layer 16A is most preferably a gold or solder (95PB-5Sn) bump, although it can be any metal which is stable in the environment, electrically conductive, and useful for interconnecting circuits of semiconductor die 30A. Some suitable materials include copper, silver, silver filled (sic) epoxy, silver-filled polyimide, silver-filled polysilioxanes, silver-filled silicone elastomers, or silver-filled silicone resins.

Therefore, the cited reference fails to establish a *prima facie* case of obviousness, and Appellant believes the 103(a) is improper.

With respect to claims 9, Applicant respectfully submits that the rejection under § 103(a) is improper because the cited references (the *Camilletti.* reference and *Bourg* reference) in view of the *Shangguan.* reference) fail to establish a *prima facie* case of obviousness. Neither of the cited references addresses the same problem as the claimed invention, or teaches all aspects claimed. Therefore, the references, either individually or in combination, cannot be used to maintain the rejection under § 103(a).

Furthermore, with respect to the § 103(a) rejections of dependent claims 3-4, 9 and 12-13, each of these claims depend indirectly from independent claim 1 or independent claim 11, each of which being patentably distinct for the reasons set forth above. As indicated at MPEP § 2143.03, if an independent claim is nonobvious under 35 U.S.C. § 103, then any claim depending therefrom is nonobvious. In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). Therefore, Applicant believes dependent claims 3-4, 9 and 12-13, when considered with their patentably-distinct base and intervening claims, to be allowable and Appellant asserts that the § 103(a) is improper and should be reversed.

Additionally, the § 103(a) rejection of claims 3-4, 9 and 12-13 over the asserted references fails to establish a *prima facie* case of obviousness by failing to provide, *inter*

Received from < 408 4749082 > at 5/16/03 12:45:01 PM [Eastern Daylight Time]

alia, a prior art teaching or suggestion of motivation for making the asserted modification of the *Camilletti* reference. A *prima facie* case of obviousness requires both: (1) complete correspondence between the asserted prior art and the claimed invention; and (2) evidence of motivation that the skilled artisan would be lead to combine the asserted teachings. In this instance, no evidence has been presented in support of the assertion that the skilled artisan would be led to modify the teachings of the *Camilletti et al.* patent with the asserted features of the *Shangguan et al.* reference.

The Office Action acknowledges that the *Camilletti et al.* reference fails to teach, *inter alia*, the claimed thickness of the diffusion barrier and metal layers. The Office Action attempts to overcome this deficiency in the teaching of the *Camilletti et al.* reference by identifying allegedly corresponding limitations in the *Shangguan* reference. However, this attempt to find complete correspondence between the asserted prior art and the claimed invention attempts only to satisfy the first component of the *prima-facie* obviousness test. No evidence of motivation has been presented for modifying the *Camilletti et al.* patent as asserted in the Office Action, and the record is devoid of any evidence whatsoever that might be construed to satisfy the above-mentioned second component of the *prima-facie* obviousness test.

In order to modify the *Camilletti et al.* reference, the Examiner must specifically identify clear and particular reasons that indicate why one of ordinary skill in the art would have been motivated to select the missing claim limitations and modify the *Camilletti et al.* reference with them. (*See, e.g.*, *In re Dembiczak*, 175 F.3d 994, 50 U.S.P.Q.2d 1614 (Fed. Cir. 1999)). In the present case, no evidence is provided in the prior art that indicates why one of ordinary skill in the art would be motivated to look to modify the *Camilletti et al.* reference with teachings of the *Shangguan et al.* reference.

The Office Action merely suggests that "It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of *Shangguan et al.* into the device taught by *Camilletti et al.* since such thickness of the diffusion barrier layer will improve the stability of the device and alleviate the interaction between the metal layers."

Such reasoning is, first of all, conclusory. No supporting evidence is provided that the stability of the resulting device would be improved, or that interaction between the metal

Received from < 408 4749082 > at 5/16/03 12:45:01 PM [Eastern Daylight Time]

layers would be alleviated. Secondly, the reasoning "will improve the stability of the device" and "alleviate the interaction between the metal layers" is too general because it could cover almost any alteration contemplated of the *Camilletti et al.* reference and does not address why this specific proposed modification would have been obvious. Thirdly, the Office Action does suggest that, other than applicant's disclosure, there is anything in either of the references that would suggest modifying the *Camilletti et al.* reference . Therefore, the rejections are improper for lack of motivation and fail to establish a *prima facie* case of obviousness. Applicant requests that the § 103(a) rejection of claims 3-4, 9 and 12-13 be removed.

In view of the above, Applicant submits that the Examiner has not made a case to support the rejections under § 103(a). Therefore, The Examiner has not met the criteria for establishing a prima facie case of obviousness in presenting the above combinations of references. The Appellant asserts that the rejections be reversed.

In the present instance, the prior art does not suggest the desirability of the combination. Accordingly, a *prima facie* case of obviousness has not been presented; therefore the §103 rejections should be reversed.

2. The rejection of claims cannot be sustained where the Examiner has failed present any specific reason for the rejection.

The Examiner (in his Final Office Action 04-DEC-2002) has made no statement of rejection in connection with claims 7, 12, 13, and 16 –20. No statement of rejection was made in connection with claims 7, 12, 13 and 16-20. Instead, the Examiner indicated that the claims were "discussed previously." Applicant submits that this statement is confusing and contrary to 35 U.S.C. §132 and M.P.E.P. §707. Specifically, any rejection maintained for these claims would be improper because the Examiner failed to give any specific reasons for the rejection. The Examiner has not responded to Appellant's traversal in the Office Action Response filed on September 3, 2002. Moreover, the rejection of these claims as stated in the previous Office Action would be improperly maintained because the Examiner failed to respond to Applicant's traversal in the Office Action Response filed on September 3, 2002, which is contrary to M.P.E.P. §707.07(f).

Received from < 408 4749082 > at 5/16/03 12:45:01 PM [Eastern Daylight Time]

Absent a specific rejection on the Examiner's part, the claims are allowable. Appellants assert that the rejection be reversed.

IX. CONCLUSION

Appellant respectfully request reversal of the rejections as applied to the appealed claims and allowance of the application.

Please charge Deposit Account No. 14-1270 (PHA 51243A) in the amount of $320.00 for filing of a Brief in support of an appeal as set forth in 37 CFR §1.17(c).

Respectfully submitted,

Date: 16-MAY-2003

By Peter Zawilski
Peter Zawilski
Registration No. 43,305
(408) 474-9063

Correspondence Address:

Corporate Patent Counsel
Philips Electronics North America Corporation
1000 West Maude Avenue
Sunnyvale, CA 94085

FAX RECEIVED
MAY 16 2003
TECHNOLOGY CENTER 2800

Received from < 408 4749082 > at 5/16/03 12:45:01 PM [Eastern Daylight Time]

APPENDIX OF CLAIMS – 09/874,606

1. A semiconductor chip having circuitry, the semiconductor chip comprising:

a metal bond pad over the circuitry and insulated on at least two sides by passivation material;

a diffusion barrier layer over the metal bond pad, at least two entire sides of the diffusion layer being insulated by the passivation material; and

a metal layer over the circuitry, the metal bond pad, the diffusion barrier layer, and at least partially over, and in contact with, a portion of the passivation material not over the diffusion barrier layer, the metal layer being configured and arranged for connecting to a wire bond, wherein the diffusion barrier layer is constructed and arranged to mitigate inter-metallic compounds forming as a reaction to the metal layer connecting to the wire bond.

2. The semiconductor chip of claim 1, wherein the diffusion barrier layer includes TiN.

3. The semiconductor chip of claim 2, wherein the diffusion barrier layer has a thickness that is at least 0.5 micron.

4. The semiconductor chip of claim 2, wherein the diffusion barrier layer has a thickness that is at least 1.0 micron.

5. The semiconductor chip of claim 1, wherein the semiconductor chip is configured and arranged as a flip chip.

6. The semiconductor chip of claim 1, wherein the metal bond pad includes aluminum.

7. The semiconductor chip of claim 6, wherein the diffusion barrier layer includes TiN.

8. The semiconductor chip of claim 7, wherein the diffusion barrier layer is further

Received from < 408 4749082 > at 5/16/03 12:45:01 PM [Eastern Daylight Time]

constructed and arranged to mitigate inter-metallic Al/Au compounds forming as a reaction to the metal layer connecting to the wire bond.

9. The semiconductor chip of claim 8, wherein the diffusion barrier layer has a thickness that is at least 0.5 micron, and the metal layer has a thickness that is at least 3 microns.

10. The semiconductor chip of claim 1, wherein the metal bond pad and the metal layer include the same type of metal.

11. A semiconductor chip having circuitry, the semiconductor chip comprising:

an aluminum bond pad over the circuitry and insulated on at least two sides by passivation material;

a diffusion barrier layer, including TiN, over the aluminum bond pad, at least two entire sides of the diffusion layer being insulated by the passivation material; and

a metal layer over the circuitry, the metal bond pad, the diffusion barrier layer, and at least partially over, and in contact with, a portion of the passivation material not over the diffusion barrier layer, the metal layer being configured and arranged for connecting to a wire bond and the diffusion barrier layer being constructed and arranged to mitigate inter-metallic aluminum-based compounds forming as a reaction to the metal layer connecting to the wire bond.

12. The semiconductor chip of claim 11, wherein the diffusion barrier layer has a thickness that is at least 0.5 micron, the metal layer has a thickness that is at least 3 microns.

13. The semiconductor chip of claim 12, wherein the diffusion barrier layer is further constructed and arranged to mitigate inter-metallic Al/Au compounds forming as a reaction to the metal layer connecting to the wire bond.

14 A semiconductor chip having circuitry, the semiconductor chip comprising:

Received from < 408 4749082 > at 5/16/03 12:45:01 PM [Eastern Daylight Time]

an aluminum bond pad over the circuitry and insulated on at least two sides by means for electrically insulating the aluminum bond pad;

barrier means, including TiN, over the aluminum bond pad, at least two entire sides of the diffusion layer being insulated by the passivation material; and

a metal layer over the circuitry, the metal bond pad, the barrier means, and at least partially over, and in contact with, a portion of the means for electrically insulating the aluminum bond pad not over the barrier means, the metal layer being configured and arranged for connecting to a wire bond and the barrier means for mitigating inter-metallic aluminum-based compounds forming as a reaction to the metal layer connecting to the wire bond.

15. A semiconductor chip having circuitry, the semiconductor chip comprising:

a metal bond pad over a portion of the circuitry;

a diffusion barrier layer over the metal bond pad; and

a metal layer over the diffusion barrier layer, the metal layer being configured and arranged for connecting to a wire bond, and the metal bond pad, the diffusion barrier layer and the metal layer all being insulated on at least two sides by passivation material;

wherein the diffusion layer is constructed and arranged to mitigate inter-metallic compounds forming as a reaction to the metal layer connecting to the wire bond, and the passivation material is constructed and arranged to be at least partially over the metal bond pad and the diffusion layer.

16. The semiconductor chip of claim 15, wherein the diffusion barrier layer includes TiN.

17. The semiconductor chip of claim 16, wherein the diffusion barrier layer is further constructed and arranged to mitigate inter-metallic Al/Au compounds forming as a reaction to the metal layer connecting to the wire bond.

18. The semiconductor chip of claim 15, wherein the diffusion barrier layer has a thickness that is at least 0.5 micron.

Received from < 408 4749082 > at 5/16/03 12:45:01 PM [Eastern Daylight Time]

19. The semiconductor chip of claim 18, wherein the metal layer has a thickness that is at least 3 microns.

20. The semiconductor chip of claim 15, wherein the semiconductor chip is configured and arranged as a flip chip.

Received from < 408 4749082 > at 5/16/03 12:45:01 PM [Eastern Daylight Time]